SUBMISSION DOCUMENT #:IEEE 802.14/97-011

PROJECT: IEEE PROJECT 802.14
Cable TV Protocol Working Group

DATE January 21, 1997

TITLE Simulation Study of ABR Service over IEEE 802.14 MAC

SOURCE:

Nada Golmie
NIST
Bldg. 820, Rm. 445
Gaithersburg, MD 20899
Phone: (301)975-4190
Fax: (301)926-9675
E-mail: nada@nist.gov

David H. Su
NIST
Bldg. 820, Rm. 445
Gaithersburg, MD 20899
Phone: (301)975-6194
Fax: (301)926-9675
E-mail: david.su@nist.gov

Mark Corner
Electrical Engineering Department
University of Virginia
Charlottesville, Virginia 22903
Phone: (804) 982-2282
Fax: (804) 982-2214
E-mail: corner@cs.virginia.edu

Jörg Liebeherr
Computer Science Department
University of Virginia
Charlottesville, Virginia 22903
Phone: (804) 982-2212
Fax: (804) 982-2214
E-mail: jorg@cs.virginia.edu

DISTRIBUTION: IEEE P802.14 WG

ABSTRACT: The goal of this contribution is to study the performance of the MAC protocol currently being specified by the 802.14 group in the presence of ATM Available Bit Rate (ABR) traffic. Preliminary simulation results of scenarios of interest are presented.

1. Introduction

An important aspect of the MAC protocol, that we identified in our contribution 96-099, is the support for higher layer traffic services, namely, ATM Constant Bit Rate (CBR), Variable Bit Rate (VBR) and Available Bit Rate (ABR) traffic classes. This effort is focused on the performance and inter-operation of the MAC defined so far by 802.14 with the ABR service. We try to provide an answer to the simple but fundamental question: Does 802.14 support the ABR service of ATM?

Note: This contribution constitutes a first attempt towards the study of the ABR flow-controlled traffic in an asymmetric access network such as HFC. Many more experiments will be required in order to provide better insights into the performance and functionality for different network situations and traffic types.

The rest of the paper is organized as follows. In section 2 we give a brief overview of the ABR flow control scheme highlighting some of its Quality of Service (QOS) requirements (that need to be supported by the MAC). In section 3 and 4 we describe the simulation environment and the test scenarios used. In section 5 we explain the simulation results obtained and in section 6 we offer some concluding remarks.

2. ABR Service Overview

The Available Bit Rate (ABR) service in ATM networks [3] is intended to carry data traffic, similar to Internet traffic, which requires a high degree of data integrity and tolerates some transfer delays. An end-to-end flow control mechanism, known as the rate-based mechanism, controls the ABR source rate as follows. A source starts sending its data at some negotiated Initial Cell Rate (ICR). Periodically, the source sends Resource Management (RM) cells along with data cells to its destination. When RM cells arrive at the destination, they are returned to the source with some flow control information, such as congestion status and expected cell rate. Any intermediate network switching node can update the feedback information contained in the RM cell on its way back to the source. Based on this feedback information, the source adjusts its rate using a number of tunable parameters. If the returning RM cell contains a congestion indication, the source decreases its Allowed Cell Rate (ACR) multiplicatively by the Rate Decrease Factor (RDF). Otherwise, the source increases its ACR additively with Rate Increase Factor (RIF).

In [3], two modes of switch behavior are defined although no complete specifications are offered for the switch mechanism; EFCI (Explicit Forward Congestion Indication) and ER (Explicit Rate). A switch in EFCI mode (EFCI switch), when in a congested state, sets the EFCI bit in the header of all data cells that are forwarded to its destination. The destination convey the congestion information back to the source by setting an appropriate field in a returning RM cell. A switch in ER mode (ER switch) is more intelligent in that it monitors its traffic and calculates an average fair share of its capacity per active virtual circuit (VC) flow. This quantity is called `explicit rate' and is given directly to the source. In comparison, an ER switch provides more efficient and fair control of the source rate than an EFCI switch.

As far as ABR QOS is concerned, the ABR service category definition [3] clearly states that no bound is required on the delay or the delay variation experienced by a given connection. There is, however, a requirement to provide a low cell loss ratio for those connections whose end-stations obey a specified reference behavior. Also, it is assumed that all connections experiencing the same congestion conditions should receive an equal (or fair) share of the network bandwidth.

If ABR traffic is carried by an HFC network, the contention at the MAC level will interfere with the rate-based mechanism. To evaluate the degree to which contention in an HFC network interferes with the feedback loop of the rate-based mechanism, we have built a simulator of a combined HFC-ATM network.

In our combined HFC-ATM network, we concentrate on the issue of fairness among ABR connections. The primary concern in our study is how well the MAC layer in HFC networks supports the ABR service. Another aspect of ABR that we consider important is the impact of delayed feedback (experienced in the HFC portion) on the ABR sources.

3. Simulation Environment

A MAC protocol conforming to the agreements reached so far by the IEEE 802.14 group [2] is implemented using the NIST ATM Network Simulator [1]. The Ternary-tree algorithm is used for contention resolution [4]. We assume that the stations request for bandwidth in contention mode only and don't use piggybacking. The number of Contention Slots (CS) and Data Slots (DS) contained in each upstream cluster is dynamically adjusted by the headend according to a simple algorithm developed at NIST that uses an estimated collision factor and the number of DS requests queued at the headend in the ratio calculation. New packets are let in the system according to $R= \min\{\max[CS, \alpha*RQ],n\}$ where CS is the number of contention minislots, α is a design parameter set to 1.9 and RQ is the request size at the headend [5]. The MAC simulation parameters are set according to Table 1. Table 2 describes the simulation parameters used for ABR sources and Table 3 describes the parameters for ABR switches. The buffers sizes of the switches are limited to 10,000 cells.

Simulation Parameter	**Values**
Number of active stations	10
Distance from nearest/furthest station to headend	25/200 km
Downstream data transmission rate	Not considered limiting
Upstream data transmission rates - aggregate for all channels	8.192 Mbits/s
Propagation delay	5 μs/km for coax and fiber
Length of simulation run	10 sec
Length of run prior to gathering statistics	10% of simulated time
Guardband and pre-amble between transmissions from different stations	Duration of 5 bytes
Data slot size	64 bytes
Minislot size	16 bytes
DS/CS size ratio	4:1
Frame size	2.27 ms (Max 160 minislots)
Maximum request size	32 data slots
Headend processing delay	1 ms

Table 1: MAC Parameters

Simulation Parameters	Values
Number of ABR sources	12 (Configuration 1) 12 (Configuration 2)
Number of CBR sources	None (Configuration 1) 5 (Configuration 2)
Nrm (Number of RM cells)	16
Available ABR Bandwidth on Congested Link	6 Mbits/s
Link Cell Rate	149.76 Mbits/s
Allowed Cell Rate (ACR)	Dynamically adjusted
Initial Cell Rate (ICR)	0.5 Mbits/s
Peak Cell Rate (PCR)	2 Mbits/s
Minimum Cell Rate (MCR)	0.149 Mbits/s
Rate Increase Factor (RIF)	0.063
Rate Decrease Factor (RDF)	1/16

Table 2: ABR End System Parameters

Simulation Parameter	Values
Explicit Forward Congestion Indication Switch-	
High Threshold	225 cells
Low Threshold	200 cells
Explicit Rate Switch -	
High Threshold	15 cells
Low Threshold	10 cells
Target Rate (TR)	10 Mbits/s
Average Factor (AVF)	1/16
Mean ACR Additive Increase Rate (MAIR)	0.015 Mbits/s
Mean ACR Reduction Factor	0.95
Measurement Interval (N)	100 cells

Table 3: ABR Switch Parameters

4. Test Scenarios

For our experiments, we design two configurations in order to study (1) fairness of bandwidth allocation among ABR connections and (2) the impact of delayed feedback on the ABR sources.
Table 4 summarizes the test scenarios used with the Fairness Configuration (1) and the Delayed Feedback Configuration (2) shown in Figure 1 and 2, respectively.

Scenario #	**Description**
Scenario 1	Fairness Configuration (1)
Scenario 2	Delayed-Feedback Configuration (2) with CBR source generation rate =0.5 Mbits/s
Scenario 3	Delayed-Feedback Configuration (2) with CBR source generation rate = 1.5 Mbits/s

Table 4: Test Scenarios

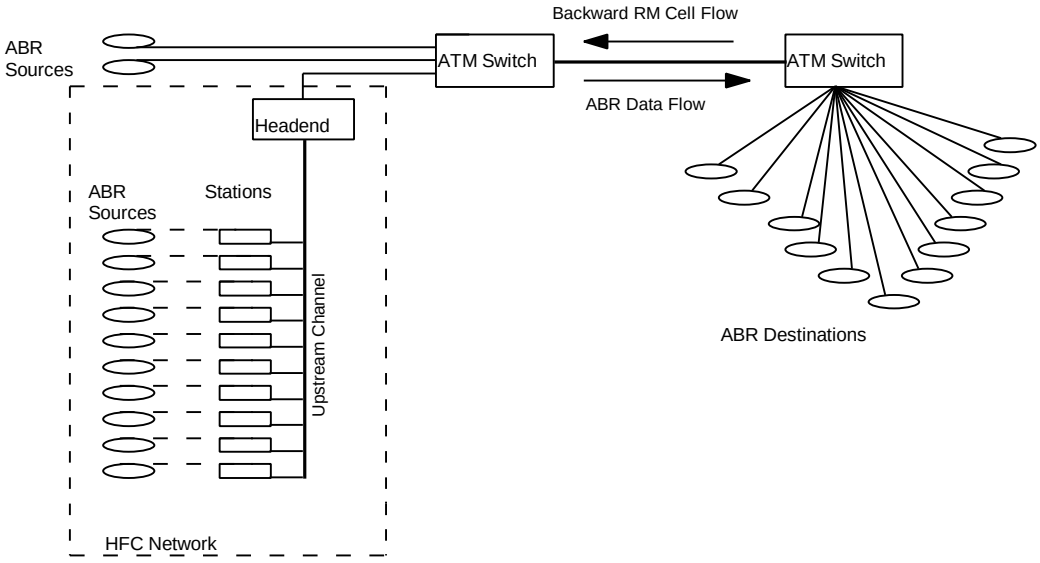

Figure 1: Fairness Configuration (1) (used for Simulation Scenario 1)

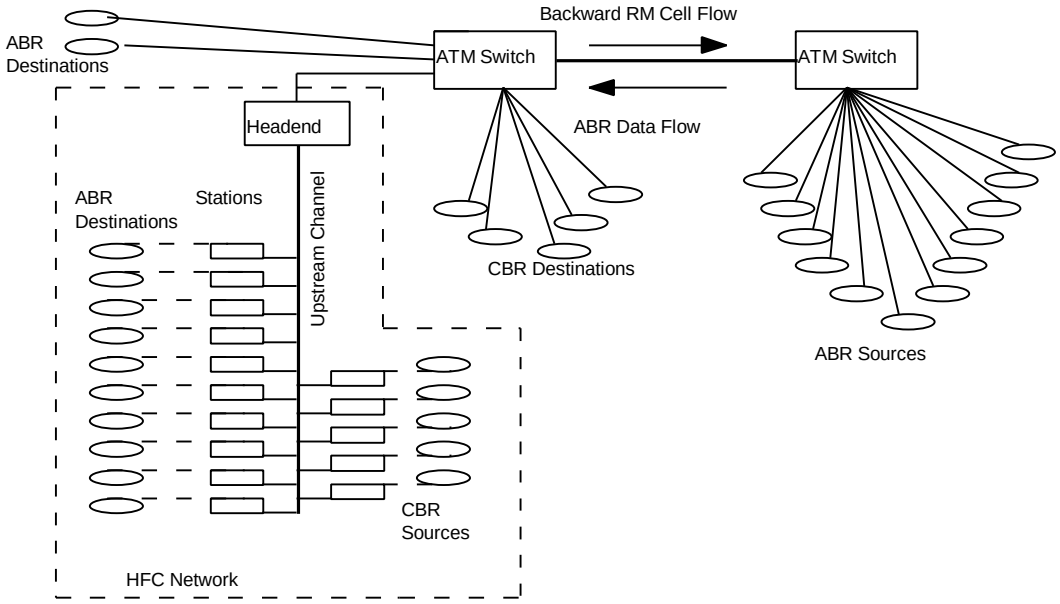

Figure 2: Delayed Feedback Configuration (2) (used for Simulation Scenario 2 and Scenario 3)

In all our simulation experiments we assume that cells are generated at a persistent constant rate for both ABR and CBR applications. This rate is set at 1 Mbits/s for the ABR applications and 0.5 and 1.5 Mbits/s for CBR applications for scenarios 2 and 3 respectively.
The measurements obtained from the simulations are as follows.

MAC Performance
1. Mean access delay (ms) histogram.

ABR Performance
1. Allowed Cell Rate (ACR) (Mbits/s) vs time.
2. Buffer Occupancy (number of cells) vs time.

5. Results

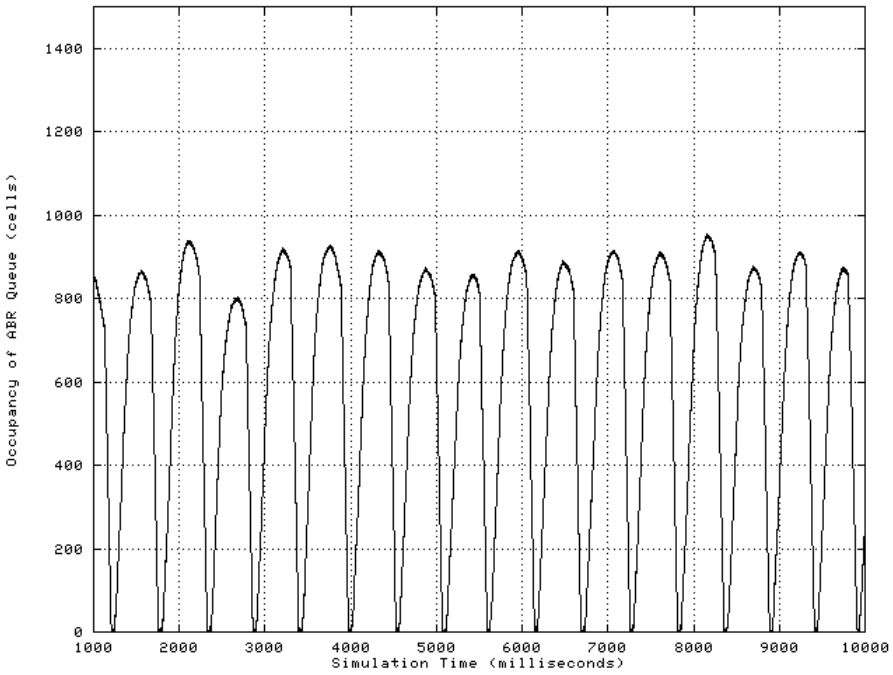

Figure 3: Scenario 1, Congested Link Switch Buffer Occupancy (EFCI Control Mechanism)

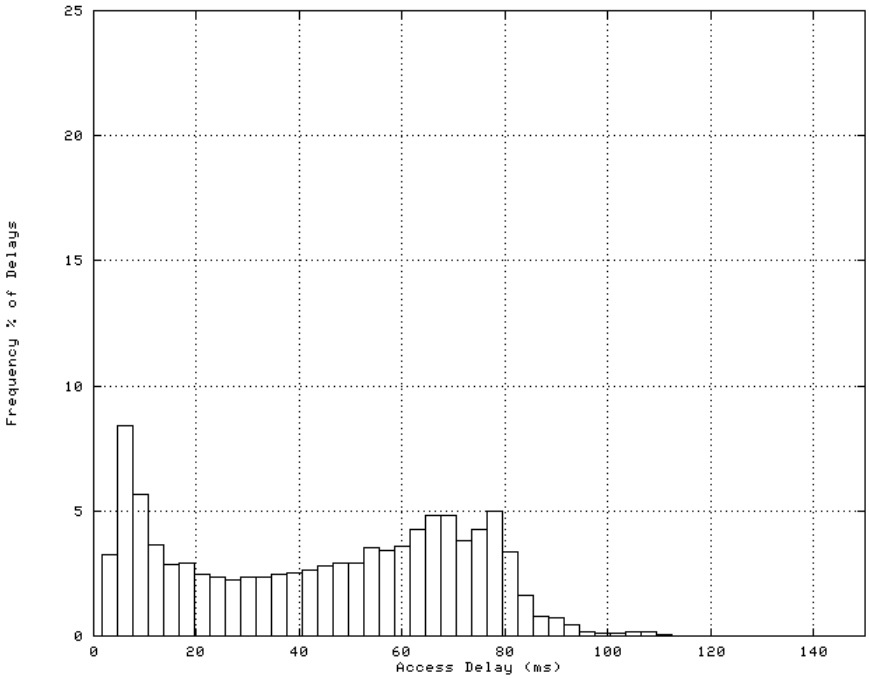

Figure 4: Scenario 1, Access Delay Histogram (EFCI Control Mechanism)

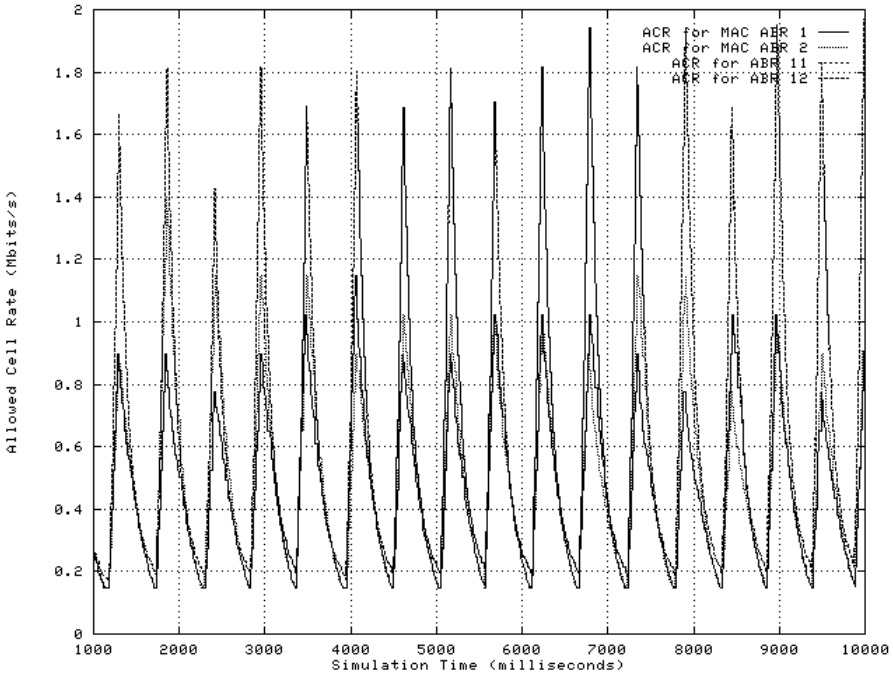

Figure 5: Scenario 1, ABR Allowed Cell Rate (EFCI Control Mechanism)

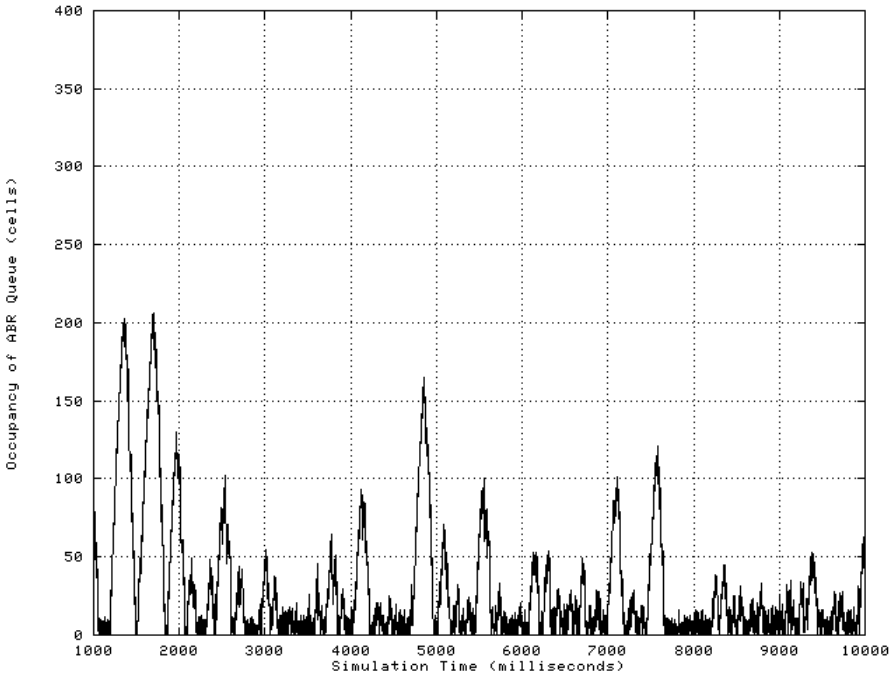

Figure 6: Scenario 1, Congested Link Switch Buffer Occupancy, (ER Control Mechanism)

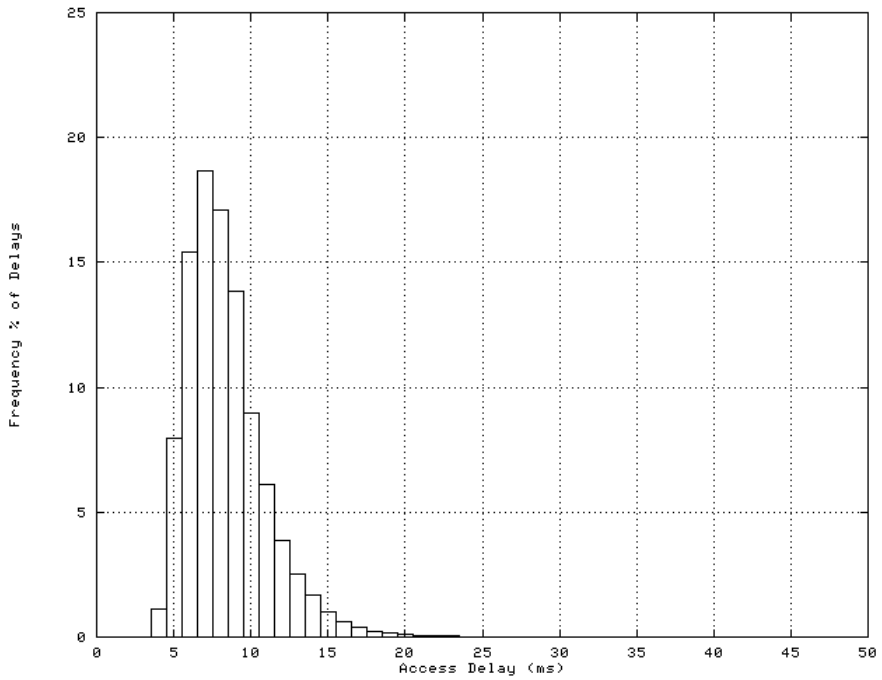

Figure 7: Scenario 1, Access Delay Histogram, (ER Control Mechanism)

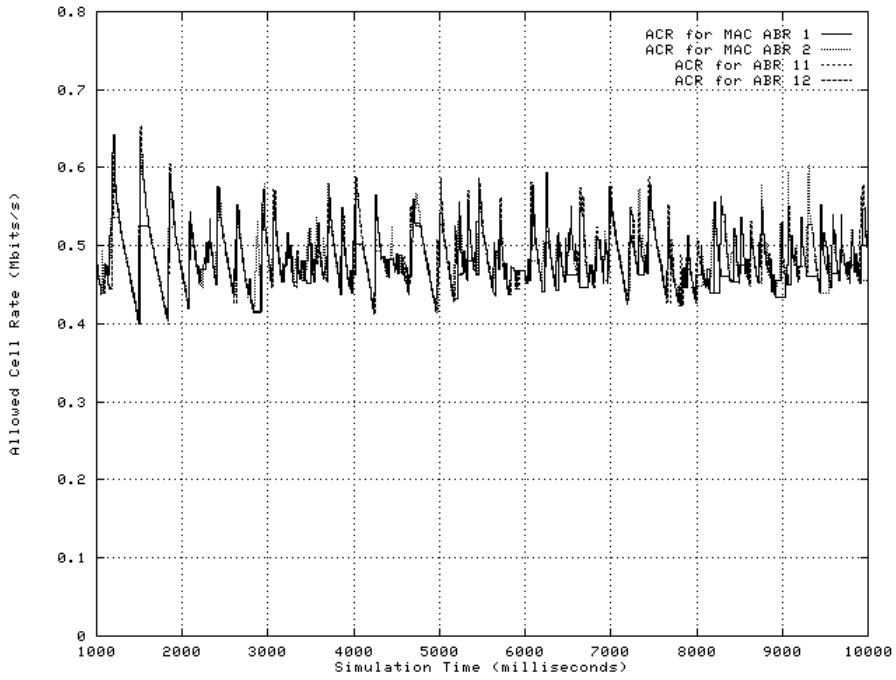

Figure 8: Scenario 1, ABR Allowed Cell Rate, (ER Control Mechanism)

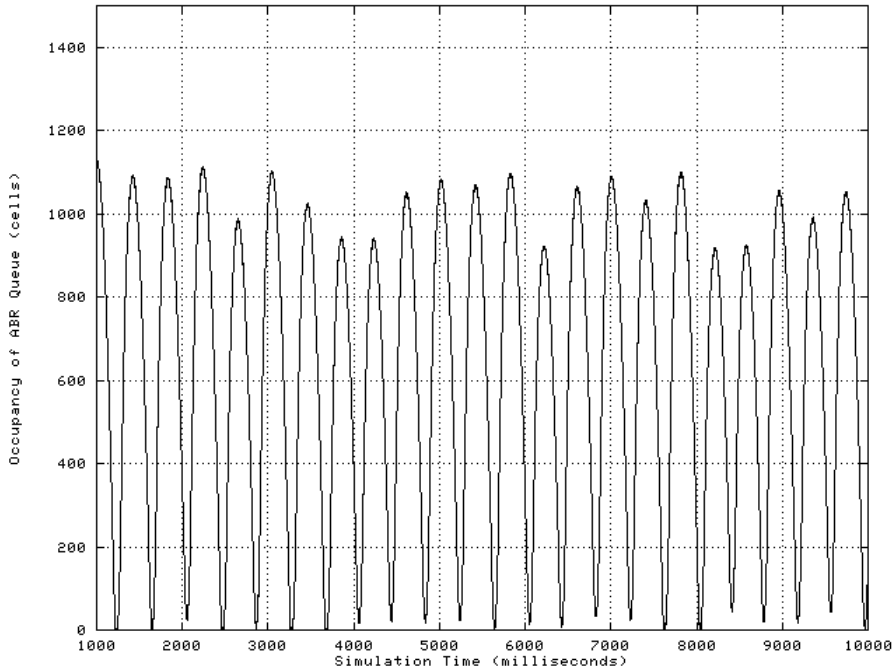

Figure 9: Scenario 2, Congested Link Switch Buffer Occupancy, (EFCI Control Mechanism)

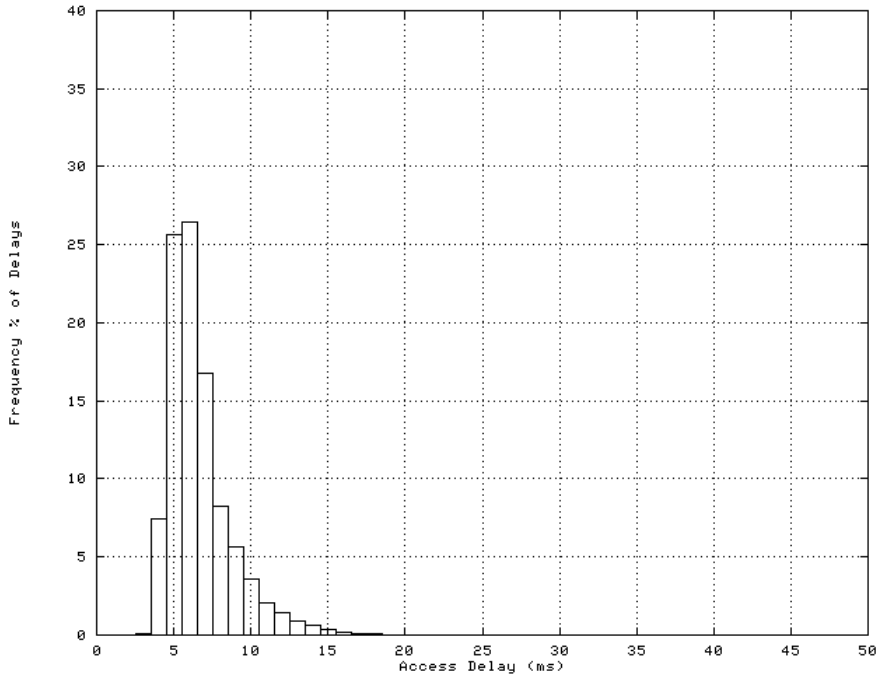

Figure 10: Scenario 2, Access Delay Histogram, (EFCI Control Mechanism)

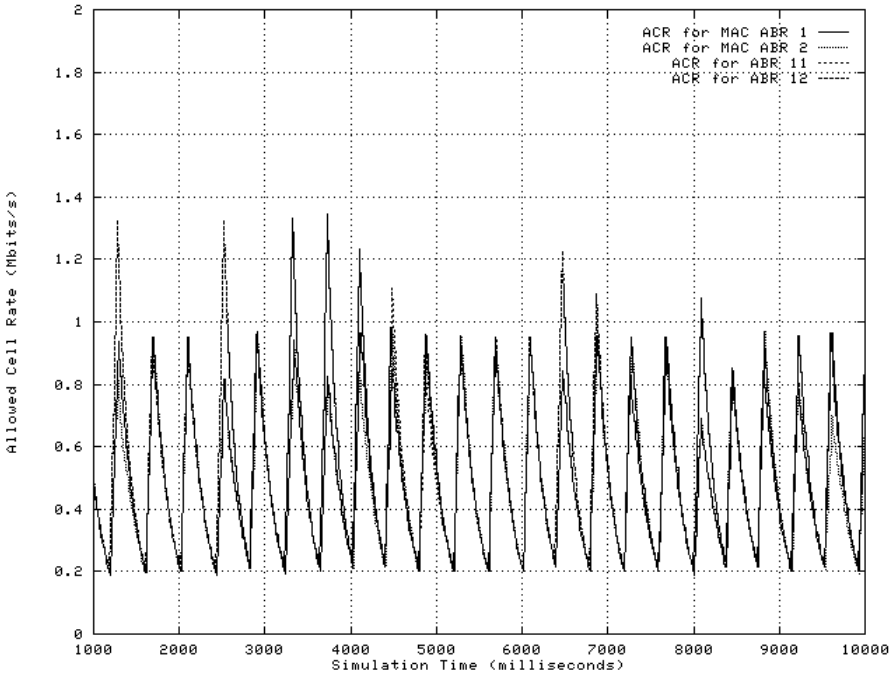

Figure 11: Scenario 2, ABR Allowed Cell Rate, (EFCI Control Mechanism)

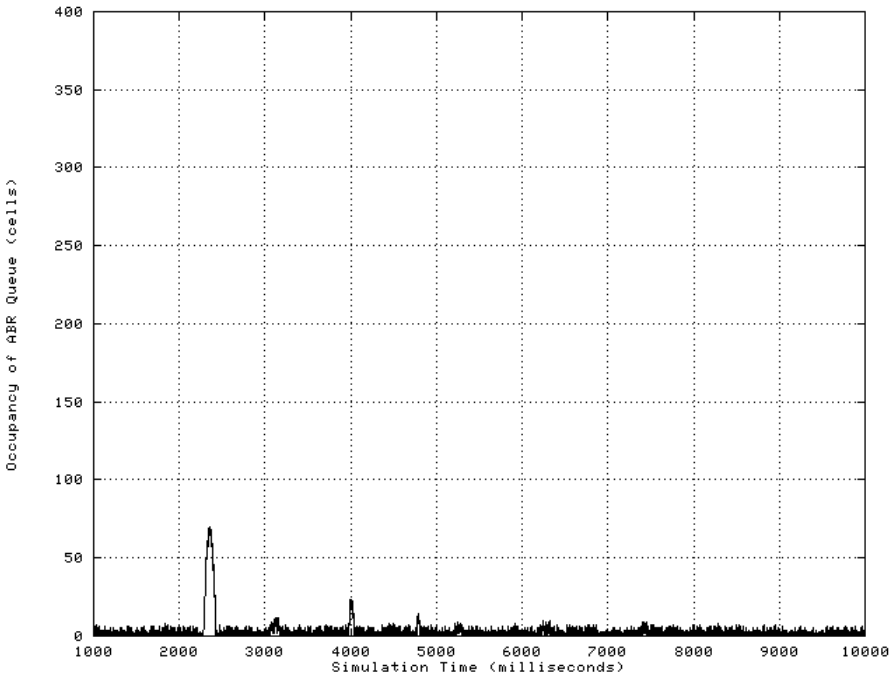

Figure 12: Scenario 2, Congested Link Switch Buffer Occupancy, (ER Control Mechanism)

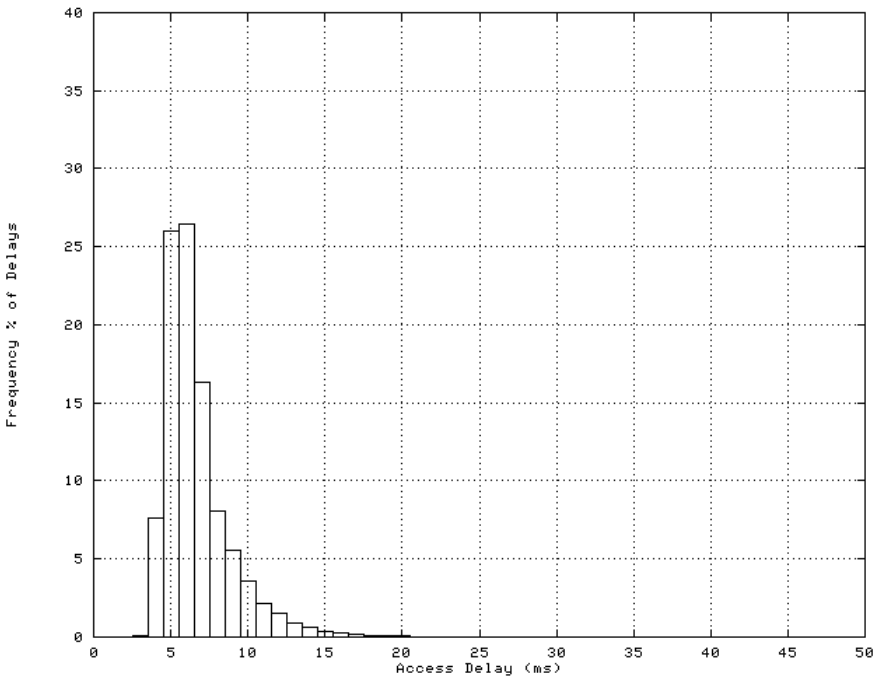

Figure 13: Scenario 2, Access Delay Histogram, (ER Control Mechanism)

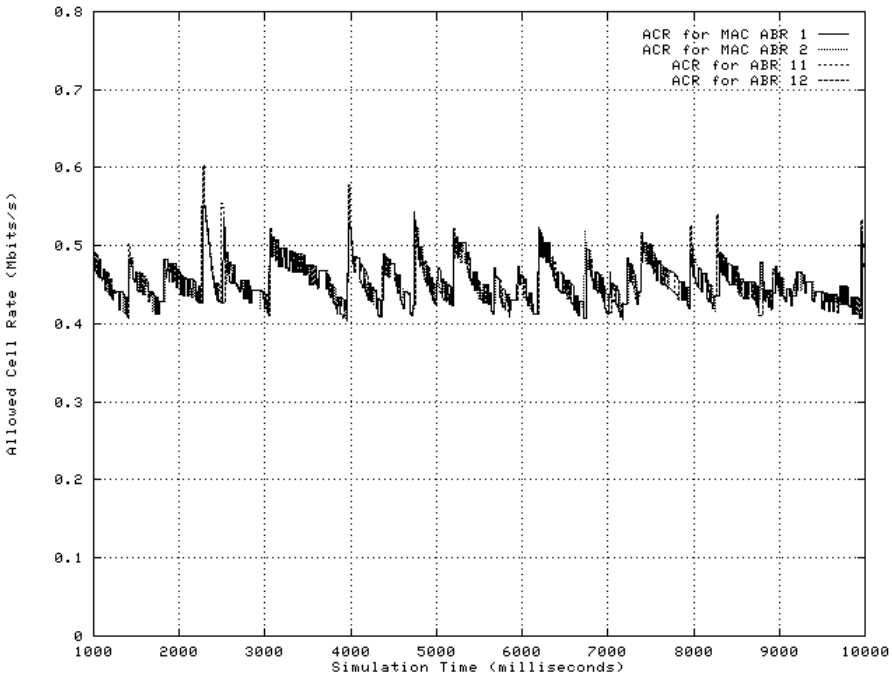

Figure 14: Scenario 2, ABR Allowed Cell Rate, (ER Control Mechanism)

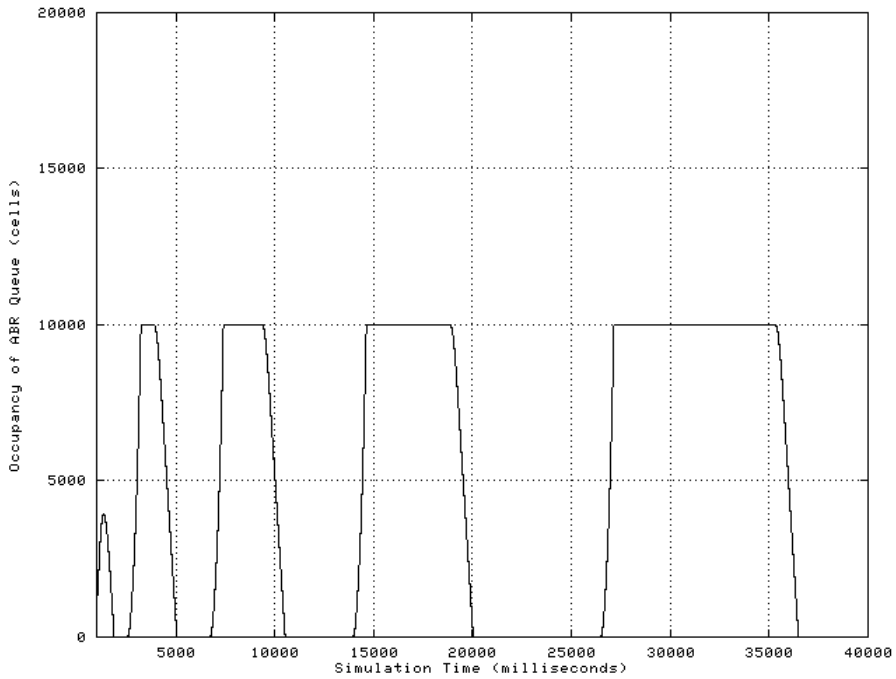

Figure 15: Scenario 3, Congested Link Switch Buffer Occupancy, (EFCI Control Mechanism)

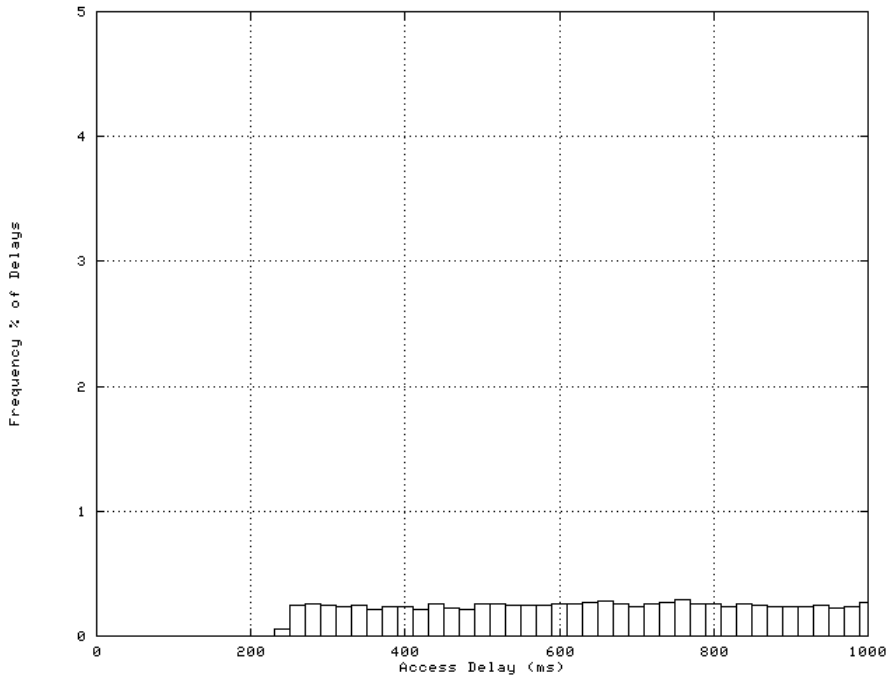

Figure 16: Scenario 3, Access Delay Histogram, (EFCI Control Mechanism)

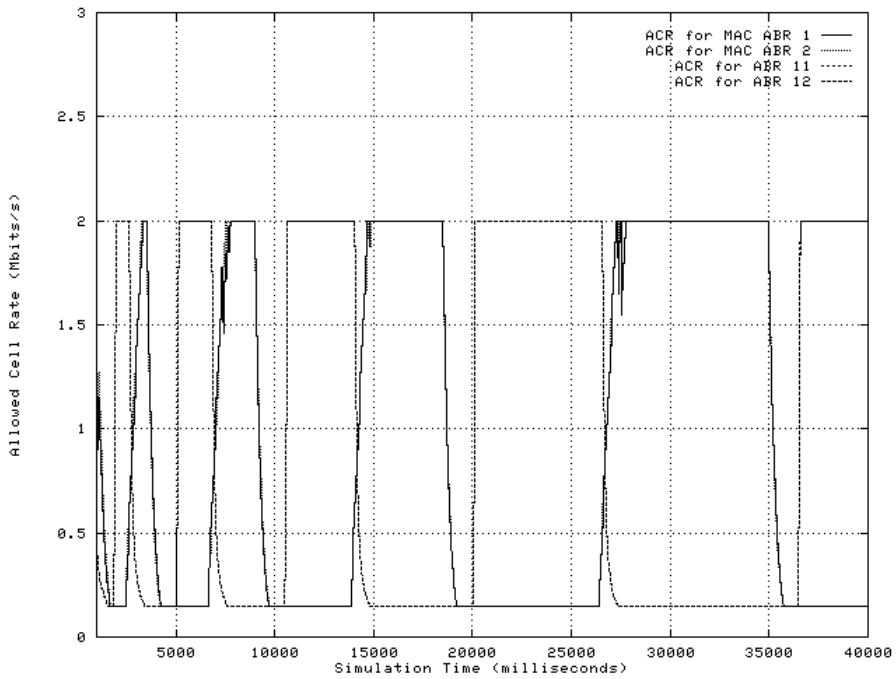

Figure 17: Scenario 3, ABR Allowed Cell Rate, (EFCI Control Mechanism)

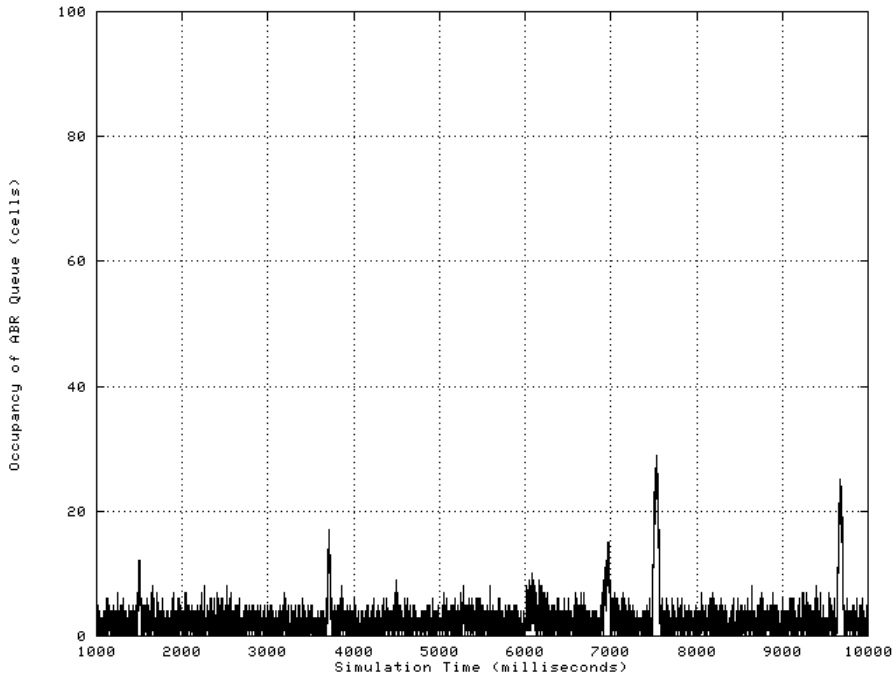

Figure 18: Scenario 3, Congested Link Switch Buffer Occupancy, (ER Control Mechanism)

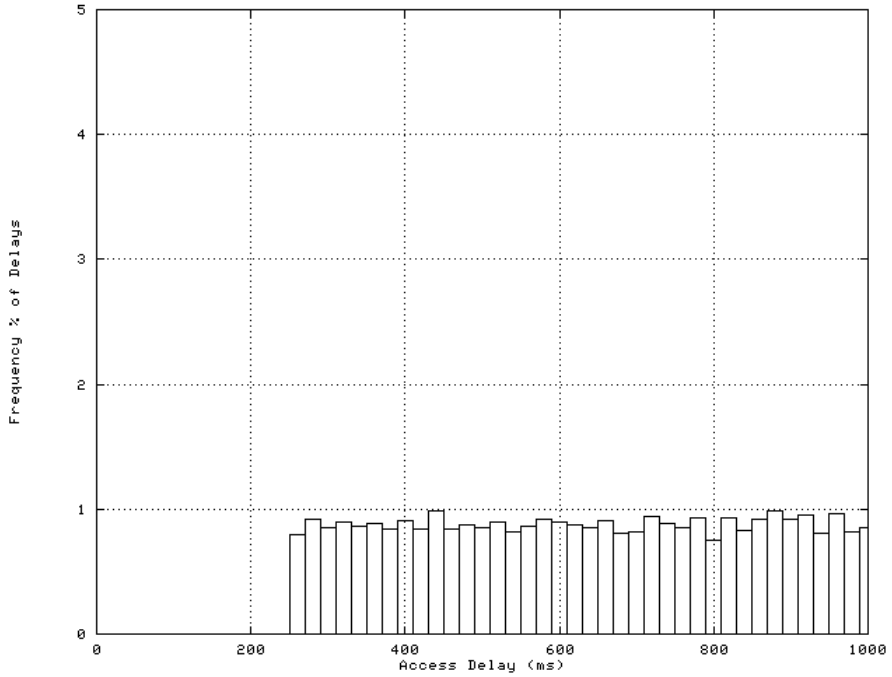

Figure 19: Scenario 3, Access Delay Histogram, (ER Control Mechanism)

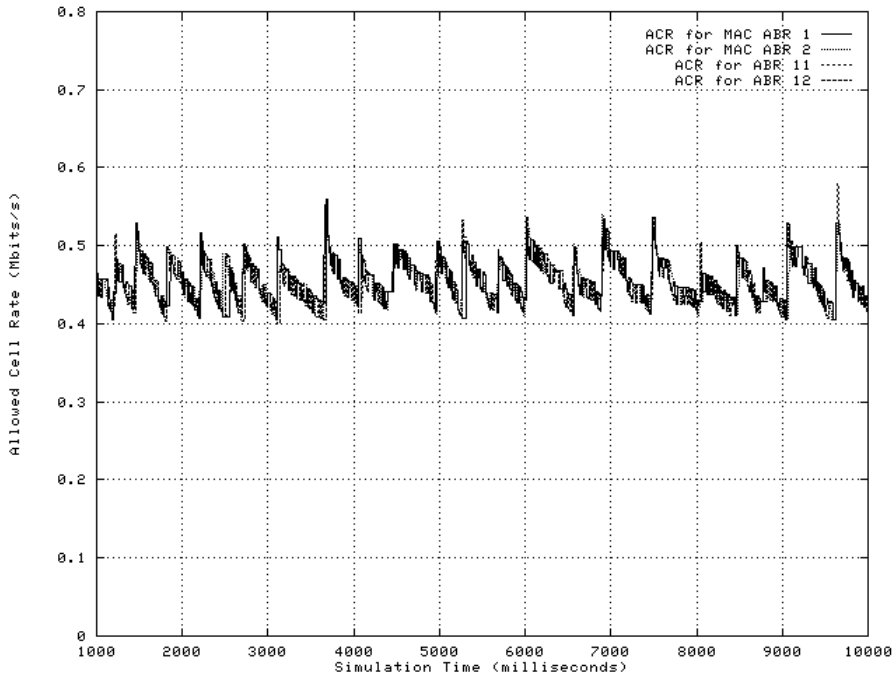

Figure 20: Scenario 3, ABR Allowed Cell Rate, (ER Control Mechanism)

Figures 3-8 show the results for Scenario 1 in terms of switch buffer occupancy, access delay and ACR rates for two different ABR switch control mechanisms, namely, EFCI and ER. In Figures 3 and 5, the amplitude and frequency of the queue oscillations and the ACR oscillations are due to the binary nature of the ABR feedback mechanism when EFCI switch control is used. The oscillations mainly depend on the round trip delay, the parameters of the increase/decrease process (RIF, RDF), the buffer threshold levels, and the Initial Cell Rate (ICR). We note that using ER control at the switch reduces the amplitude and frequency of the buffer and ACR oscillations (Figure 6 and 8). Note that the access delay variations with EFCI control, shown in Figure 4, are rather large and have a heavy tail distribution. The values observed in Figure 4 are in the 4-130 ms. In contrast, Figure 7 shows that using ER control results in observed access delays less than 25 ms. The difference of the access delays between EFCI and ER is due to the large feedback delays of the EFCI control mechanism.(The feedback delays of EFCI control are evidenced by the high buffer occupancy of the congested link switch shown in Figure 3.)
From the instantaneous ACR plot in Figure 5 and 8, we note that fairness among the different ABR applications, in both a pure ATM environment (ABR 11, and ABR 12) and HFC environment (MAC ABR 1 and MAC ABR 2) is achieved. The ACR rates oscillate around the expected rate of 0.5 Mbits/s.

The results for Scenario 2 are illustrated in Figure 9-14. The ACR and the queue oscillations are as expected (Figure 9,11, 12, and 14). The access delays are the almost identical for EFCI and ER switch control (Figure 10 and 13). This is due to the under-loading of the upstream channel where only backward RM cells and light CBR traffic is transmitted.

Results for Scenario 3 are shown in Figure 15-20. In this scenario, the upstream channel is overloaded due to CBR traffic that contends for upstream channel resources. Note in Figure 15, that the backlog of the ABR queue is limited to the maximum buffer size of 10,000 cells. Since the upstream channel is congested, the backward RM cells that are transmitted on the upstream channel are being delayed at the MAC layer. This increase of the MAC delay causes a rather large cycle time in the ACR oscillations for both EFCI and ER switch control (almost 4 seconds in Figure 17 with EFCI control and 0.5 seconds in Figure 20 with ER control). As expected, the large cycle times result in long access delays, as shown in Figure 16 and 19.

6. Concluding Remarks

The preliminary results presented in this contribution clearly indicate that the 802.14 MAC protocol supports the ABR service of ATM. The presented simulations show the degree to which MAC contention on the upstream channel interfere with the rate control mechanisms of ABR. However, many more investigations are needed to gain full insight into the interdependencies between the traffic control mechanisms in HFC and ATM.

References

[1] N. Golmie et. al. “The NIST ATM Network Simulator: Operation and Programming,” *National Institute of Standards and Technology, Internal Report* 5703, August 1995.
[2] Draft Supplement to IEEE Std 802.14, 802.14MAC/V1.0, November 30, 1996.
[3] ATM Forum Traffic Management Specifications 4.0, April 1996.
[4] B. McNeil et. al, “Implementation Overview of Tree-Based Algorithm “, Contr. No. IEEE 802.14/96-246, IEEE 802.14 Working Group (WG) Meeting, November 1996
[5] N. Golmie et. al, “ New Packet Admittance Policies for IEEE 802.14 MAC Protocol,” Proceedings of the Fourth International Conference on Optical Communications and Networks, Paris, France January 1997.