Lab 2: Common-Source Amplifiers

Introduction

The common-source stage is the most basic amplifier stage encountered in CMOS analog circuits. Because of its very high input impedance, moderate-to-high gain, low noise, bandwidth and simplicity, the common-source amplifier finds different applications ranging from sensor signal amplification to RF low-noise amplification. Good understanding of this amplifier stage is essential for the analysis and design of more advanced circuits, such as differential amplifiers, which you will encounter later in this course.

In this lab, you are going to design, simulate, and implement NMOS- and PMOS-based common-source amplifiers with resistive loads and a CMOS inverter amplifier, as shown in Figure 1. The CMOS inverter is biased for operation as a linear amplifier by connecting a large resistor ($>$ 300-kΩ) between its input and output. This circuit is becoming very popular in nanoscale CMOS technonology as a low-noise, broadband amplifier and as a power amplifier output stage. The three amplifier stages will be designed for different requirements such as gain, linear voltage swing and supply voltage. Note that the vendor does not provide the gate length and gate width of the MOSFETs used in this lab. Therefore, the only design parameters you have available for the MOSFETs is V_{GS} and V_{DS}. You will not be able to determine the current density at which the transistors operate and whether or not the square law applies at each bias current.

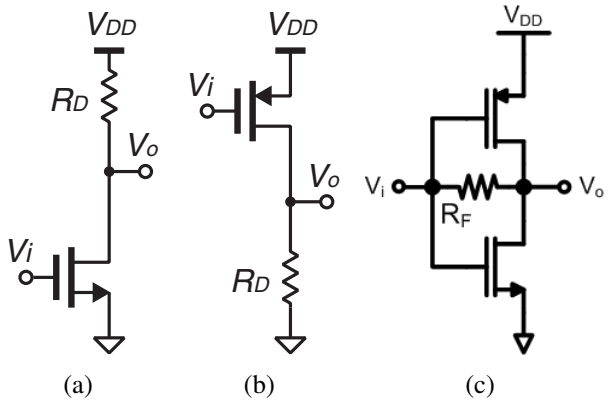

Figure 1: (a) NMOS and (b) PMOS common-source amplifiers with resistive loads. (c) CMOS inverter amplifier with resistive feedback for bias point stabilization.

Preparation

Go through the following preparation steps.

1. Find the expressions for the small-signal gain of the NMOS and PMOS common-source amplifiers shown in Figure 1 designed for the maximum output swing with an arbitrary I_D. The gain should be expressed in terms of only V_{DD} and V_{ov} without any numerical values. Assuming that the square law applies and that the transistors are in the active region. Assume that r_o is much larger than R_D and therefore it can be ignored.

2. Design common-source amplifiers for the criteria shown in Table 1. Perform hand analysis to fill in the blanks in Table 1 using the device parameters shown in Table 2.

3. Perform a DC operating point simulation for the amplifiers designed above. Note that the transistor models used in simulation are far more complicated and accurate than the simple square law used for hand analysis. Therefore, some deviation from the hand analysis comes with no surprises.

4. Perform a DC sweep to plot the transfer characteristics of each amplifier stage. Plot V_o, I_D, and $dV_o/dV_i(=A_v)$ versus V_i in the same graph window. V_i should be swept from 0 V to V_{DD}.

5. Label and comment on the plots to clearly show the the small-signal gain (A_v), V_i, and output swing for the I_D specified in Table 1.

6. Perform a transient simulation to obtain the output voltage waveforms: V_o versus time. Use a sinusoidal voltage source at 1 kHz with 10-mV_{pp} amplitude as the input source. Make sure that the DC input and output voltages are the same as those found in the previous step. Verify the small-signal gain found in the previous step.

7. Perform a transient simulation for different input amplitudes to show V_o versus time. Use a sinusoidal voltage source at 1 kHz with 100-500mV_{pp} amplitude as the input source. Make sure that the input and thus the output are biased at the voltages found in the previous step. Find the maximum linear output voltage swing.

8. Organize the results for presentation to your TA.

Lab

Perform the following for the first two common-source amplifiers designed by hand analysis. A minimum parts list for this lab is shown in Table 3. This is the absolute minimum. You may bring more parts for your convenience and backup.

Table 1: Hand analysis table

V_{DD} (V)	Type	V_A	Gain	Swing (V_{pp})	V_{ov} (V)	I_D (A)	g_m (A/V)	V_o (V)	R_D (Ω)	A_v (V/V)
5.0	NMOS	80 V	max			1 m				
5.0	PMOS	-19 V	max			0.5 m				
5.0	CMOS	-	max		-					
1.2	NMOS	80 V	max	0.2		0.5 m				

Table 2: NMOS and PMOS device parameters

Type	Device	V_T (V)	$\mu_{n/p}C_{ox}W/L$ (mA/V^2)
NMOS	ALD1101	0.71	4.49
PMOS	ALD1102	-0.65	-2.10

1. Measuring the transfer characteristics: V_o versus V_i

Repeat the following for the first two common-source amplifiers designed in the preparation.

1. Implement the common-source amplifier on the breadboard. Connect a 50-Ω resistor across the input and the ground as shown in Figure 2 . This resistor is important for the voltage reading of the signal generator to be correct. Most of the signal generators have a 50-Ω output impedance and the voltage reading is correct only if its load is 50 Ω. **You will need this 50-Ω termination many times in future labs when you use a signal generator although it won't be explicitly shown in lab manuals.**

2. Configure the signal generator for a triangular wave with 0 V to V_{DD} swing at 100 Hz. Make sure to do this step without connecting the transistor to the signal generator but with the 50-Ω resistor connected, as an excessive gate voltage can permanently damage the transistor.

3. Connect the input signal to the transistor and measure the input (V_i) and output (V_o) simultaneously using both channels of the oscilloscope. Use the input signal as the trigger source. Adjust the horizontal scale to display roughly two periods of the triangular wave and adjust the vertical scale of each input to maximize the displayed signal swing without clipping. Make sure that V_i swings from 0 V to V_{DD}.

Table 3: Minimum parts list

Part	Description	Quantity
ALD1101	NMOS transistor	1
ALD1102	PMOS transistor	1
-	10-kΩ multi-turn potentiometer	1
-	$>$ 300-kΩ resistor	1

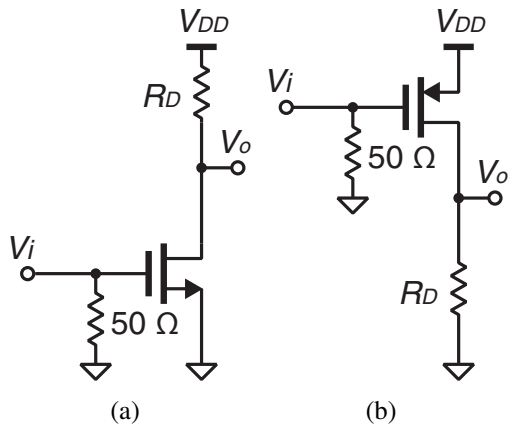

Figure 2: (a) NMOS and (b) PMOS common-source amplifiers with a 50-Ω input impedance.

4. Enable the XY plot mode of the oscilloscope to plot V_o versus V_i. Determine and record the input and output bias voltage that meets the I_D requirement in Table 1, and calculate the small-signal gain around that point. Sketch a V_o versus V_i curve and label important points. How does this compare with the simulation and hand analysis?

5. Organize the results for presentation to your TA.

2. Small signal and large signal testing under sinusoidal excitation

Repeat the following for the first two common-source amplifiers designed in the preparation.

1. Disconnect the signal source from the circuit, and configure the signal source for 1-kHz 10-mV_{pp} sinusoid.

2. Place the input bias circuit for the NMOS and PMOS common-source amplifiers on the breadboard as shown in Figure 3, and tune the potentiometer for the input bias voltage found in part 1. **This input bias circuit is used many times in future labs** so make sure you feel comfortable with it. The CMOS amplifier is self-biased through the feedback resistor, therefore you need not connect any other bias network.

3. Connect the signal source to the input of the amplifier on the breadboard and display both the input and the output signals of the amplifier stage on the oscilloscope. How does the gain compare with that obtained from hand analysis and from simulation? Which of the three amplifier stages has the highest gain and the largest output voltage swing for a given V_{DD} value?

4. Organize the results for presentation to your TA.

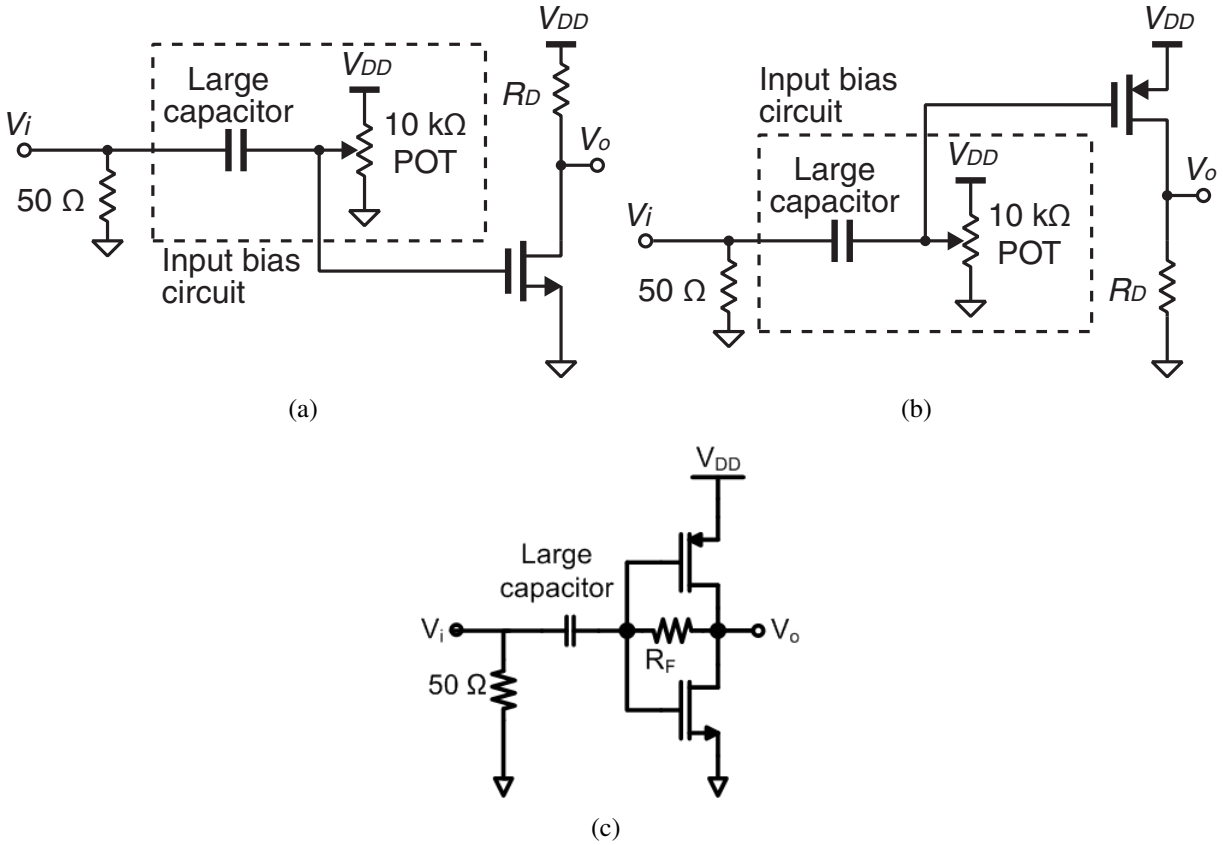

Figure 3: (a) NMOS, (b) PMOS and c) CMOS inverter common-source amplifiers with bias circuits and input DC-blocking capacitor.