# Distortion and Noise Performance of Bottom-Plate Sampling Mixers

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*Abstract*— **Distortion and noise due in a bottom-plate sampling mixer is analyzed. The method of Volterra series is applied in the analysis of harmonic distortion, which combines the effects of continuous time, time varying, and sampling distortions. Frequency domain analysis is applied in the analysis of thermal noise. The method of stochastic differential equation is used to solve for LO noise. These two noise effects, when combined with LO jitter, give a complete noise picture. The analysis is performed in sampled data domain. Explicit formulas are given to guide the design of bottom-plate sampling mixers.**

## I. Introduction

The recent surge of interest in wireless digital communication and the advance of VLSI technology have made the implementation of monolithic CMOS wireless receivers feasible. In the receiver chain, it is desirable to perform front-end operations such as mixing and A/D conversion as early as possible, ideally on the RF signal directly [1], [2], [3]. However, early conversion also puts stringent performance requirements on the A/D converter which has to operate at the much higher RF frequency. At high frequency, both distortion and noise become significant problems. One of the key circuit elements in A/D conversion is the front-end track-and-hold sampling mixer that simultaneously performs sampling and mixing. Mixer linearity often limits the total harmonic and intermodulation distortion and the mixer is often a major contributor of noise. In this paper, we will concentrate on the distortion and noise analysis of a passive MOS-based bottom-plate sampling mixer.

Distortion is produced by circuit nonlinearity, and it can be analyzed using the nonlinear theory of Volterra series. The time invariant Volterra series can be used to analyze mixer distortion in the case where the LO (local oscillator) waveform is a perfect square wave [4] [5]. In the case where the LO waveform has a finite slope, Volterra series can be extended to time varying cases and applied in sampled data domain to solve for time varying distortion [6]. In addition, there is also distortion due to sampling error. In this paper, all three sources of distortion will be investigated for the bottom-plate sampler.

Noise is another major consideration in the design of sampling mixers. Noise may come from the external RF port, the switching LO (local oscillator) port, or from within the mixer itself. Noise analysis can be done in frequency domain in cases where the circuit is linear and time-invariant. For the sampling mixer, this approach is applicable to the analysis of intrinsic and external RF noises, but not to LO noise. In the case of LO noise, the system is neither linear nor time-invariant due to the switching nature of the LO waveform. In this paper, we will adopt a time domain approach based on solving a stochastic differential equation (SDE). The method of SDE's for circuit noise analysis was used in [7] from a circuit simulation point of view. Their approach is based on the linearization of SDE's about its simulated deterministic trajectory. In this paper, we will use a different approach from which an analytical solution to the SDE will be obtained.

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## II. Sampling Mixers

A single switch sampling mixer consists of a MOS transistor followed by a sampling capacitor (Fig. 1). The input $V_{RF}$ is at RF or IF frequency. The output $V_o$ is sampled and held on the capacitor when the LO voltage applied at the gate goes low. The output is considered in the sampled data domain. This circuit not only serves

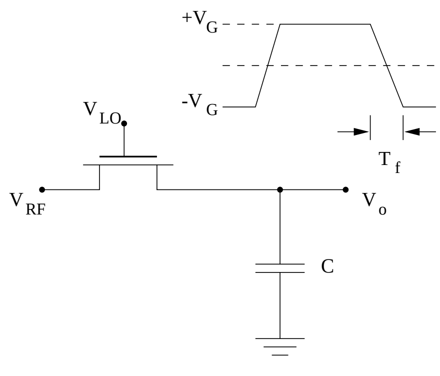


Fig. 1. A Simple Sampling Mixer

as a track-and-hold front-end to the A/D conversion, but also acts as a mixer that mixes down RF or IF signals to the baseband. If the input frequency is $\omega_{RF}$ and the LO frequency is $\omega_{LO}$, frequency components at $\omega_{RF} - n \cdot \omega_{LO}$ are present at the output.

This simple circuit suffers from the charge injection problem. When a MOS transistor turns off, the charges that compose the inversion layer have to be injected to either the source or the drain, depending on their relative impedance. In the simple scheme of Fig. 1, the impedance of the output side, $1/j\omega C_s$, is comparable to input impedance at high frequency, hence the sampling capacitor attracts extra charges that disturb the output signal level. The bottom-plate sampling scheme eliminates such problem (Fig. 2). In this scheme, the bottom

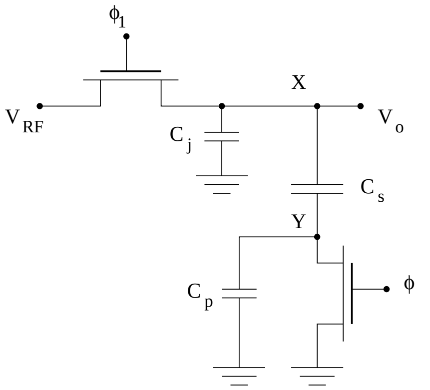


Fig. 2. Bottom Plate Sampling

transistor turns off first, then the top transistor turns off. The output is taken as the voltage across the sampling capacitor $C_s$. In the figure, $C_j$ and $C_p$ are included as junction capacitance of top and bottom transistors, respectively, which are typically much smaller than $C_s$. As the bottom transistor turns off, the impedance of top side is larger than the ground impedance, so charges are injected to the ground. As the top transistor turns off, the impedance of the output side is mainly due to the small parasitic capacitance, $1/j\omega(C_p+C_j)$, which is large compared to the impedance of the input side, so charges are injected back to the input. In either case, very little extra charges are dumped onto the sampling capacitor, hence avoiding the charge injection problem.

To see that this circuit operates as a sampling mixer, we can model the transistors as simple switches. As the bottom transistor turns off, it fixes the amount of charge on the capacitor $C_s$, when the top transistor turns off, it fixes the voltage levels of X and Y. It can be shown that the output voltage is a linear combination of two parts:

$$V_{out} = \left(\frac{C_s}{C_s+C_p}\right) \cdot V_{bottom} + \left(\frac{C_p}{C_s+C_p}\right) \cdot V_{top}, \tag{1}$$

where $V_{bottom}$ is the voltage at node X when bottom switch turns off, and $V_{top}$ is the voltage at node X when top switch turns off.

## III. Distortion of Bottom Plate Mixers

The MOS transistor device equation is nonlinear, which causes distortion in the output waveform. The main distortion quantity of interests is intermodulation distortion $\mathrm{IM}_3$, which is the magnitude of the sinusoid $sin(2\omega_1 t - \omega_2 t)$ in the output for inputs at frequencies $\omega_1$ and $\omega_2$. The distortion for the simple structure of Fig. 1 has been completely worked out using Volterra series [6]. Distortion is found to have three components, that due to the continuous time operation,

$$IM_3 = \frac{A^2}{4} \cdot \frac{j\omega C}{K(V_G - V_t)^3}, \tag{2}$$

that due to the time varying LO waveform,

$$IM_3 = \frac{3A^2}{4} \cdot \omega^3 \cdot \sqrt{\frac{C}{K}} \left(\frac{T_f}{V_G}\right)^{5/2} \cdot 0.234. \tag{3}$$

and that due to sampling error,

$$IM_3 = \frac{A^2}{32} \cdot \omega^2 \cdot \left(\frac{T_f}{V_G}\right)^2, \tag{4}$$

where the input is assumed to be a sinusoid $A \cdot sin(\omega t)$, $K$ is the device constant $\mu C_{ox} W/L$, $V_t$ is the threshold voltage of the MOS, $C$ is the sampling capacitor, and $V_G$, $T_f$ are as shown in Fig. 1. Continuous time distortion is calculated by assuming a perfect square waveform LO. Time varying distortion is calculated for a LO waveform with a non-zero fall time. In this case, distortion is calculated by solving a differential equation with non-constant coefficients for each sample point, which are then combined in sampled data domain by taking advantage of the system periodicity. This effectively transforms a time varying system to the time invariant case. Both continuous time and time varying distortions are due to the nonlinear conductance of the MOS transistor which is signal modulated. Sampling distortion is due to signal dependent sampling, which is independent of MOS nonlinearity. Typically, continuous time distortion dominates at small LO fall time, sampling distortion dominates at large LO fall time, and time varying distortion is usually smaller than either of the other two sources.

The same analysis applies to the bottom-plate sampler case. As seen in (1), the total distortion of the bottom-plate sampler is a linear combination of two parts, each of which contains distortion from the three sources.

Let us first consider distortion when the bottom switch turns off. First, notice that the sampling error is small, because the source and the drain of the bottom switch are kept constant at the ground level, which eliminates signal dependent sampling. Next, we need to calculate continuous time distortion. To obtain an exact solution, we have to solve two coupled differential equations, which is cumbersome. However, in this case, we can argue that since both the source and the drain side of the bottom transistor are kept at ground level, its distortion contribution is negligible. Therefore continuous time distortion for the bottom-plate sampler is mainly due to top plate, which reduces the problem to the single switch case as in equation (2).

We also need to consider time varying distortion when bottom switch turns off. This is difficult because we have a second order differential equation with non-constant coefficients. However, as the bottom switch turns off its resistance increases and eventually reaches infinite, but the resistance of the top transistor remains small, so we can replace the top switch by a short, and simplify the problem to a one which has only one capacitive node. Following the methodology developed in [6], time varying distortion may now be derived in sampled data domain. The final expression for time varying distortion turns out to be exactly same as the single switch case, except $C$ in (3) is replaced by $C_s + C_p$. This time varying distortion is much smaller than continuous time distortion, so as the bottom switch turns off, distortion accumulated is mainly due to the continuous time operation as expressed in (2).

Now, we need to calculate distortion when the top switch turns off. The situation is identical to the case in Fig. 1, since the bottom switch is off. Equations (2)-(4) apply. In this case, continuous time distortion is much smaller since the capacitor is much smaller. Therefore, sampling distortion is the dominate factor.

Total distortion is a linear combination of the above two factors:

$$\begin{aligned} IM_3 &= \left(\frac{C_s}{C_s + C_p}\right) \cdot \frac{A^2}{4} \cdot \frac{j\omega(C_s + C_j)}{K_1(V_G - V_t)^3} \\ &\quad + \left(\frac{C_p}{C_s + C_p}\right) \cdot \frac{A^2}{32}\left(\frac{\omega T_f}{V_G}\right)^2, \end{aligned} \tag{5}$$

where $K_1$ is the device constant of the top switch. We note here that subsampling has no effect in the distortion analysis since distortion is calculated for each sample point in discrete domain. The major difference between bottom-plate and the single switch case is that the distortion due to sampling error (when top switch turns off) is lessened by a factor of $C_p/(C_s + C_p)$. Therefore, distortion due to non-zero fall time is much less a problem in bottom-plate sampling than in the simple case of Fig. 1. So, bottom-plate sampling is advantageous also from distortion point of view. From (5), we also see that the size of the top switch is much more important than the size of the bottom switch. To keep distortion minimum, the top switch needs to be large, while the bottom switch can remain relatively small.

## IV. Noise in Bottom Plate Mixers

Much like distortion, there are also three sources of noise in a mixer. There is thermal noise from either the RF port or from the device intrinsic noise, there is noise due to fluctuation in LO, which is coupled into the output, and there is noise due to LO jitter. Each of the three factors must be analyzed separately.

We first analyze noise in the single switch case (Fig. 1). Intrinsic and RF noise may be calculated using frequency domain methods. First, consider the sampling mixer with its gate voltage fixed at high. This corresponds to a continuous time-invariant non-mixing operation, where the MOS switch and the capacitor form a lower pass filter with filter bandwidth approximately equal to $g/C$, where $g = K(V_G - V_t)$ is the MOS ON-conductance. This neglects the square law nonlinearity in the MOS device equation, which is justifiable because the nonlinearity must be small by design. Suppose that both input and intrinsic noise is white with combined two-sided power spectral density at $\sigma^2 = 2kT(R_{inp} + R_{mos})$, where $R_{inp}$ and $R_{mos}$ are the equivalent input noise resistor and intrinsic noise resistor respectively. Then, the noise at the output has a low pass shaped power spectral density with -3dB frequency equal to the filter bandwidth. The total noise power at the output is:

$$E[N_t^2] = \frac{kT}{C}\left(1 + \frac{R_{inp}}{R_{mos}}\right), \tag{6}$$

where $N_t$ is the output noise process. The noise variance applies to every sample, and it is independent of sampling rate. The low pass shape of the power spectral density also means that in time domain correlation between consecutive samples decreases exponentially with the time constant equal to that formed by the MOS and the capacitor. Since the time constant is designed to be much smaller than sampling period to allow accurate tracking, discrete samples can be considered independent and identically distributed (iid), whose discrete power spectral density is folded into the frequency band from 0 up to $f_s/2$, where $f_s$ is the sampling frequency. Consequently, in the subsampling case, although noise variance stays the same, the amount of noise in the signal band increases by the subsampling ratio.

We also need to consider noise from the LO port. There are two distinct mechanisms by which noise at LO can contribute to total noise at the output. First, due to the noise at the LO port, the time at which sampling occurs is random. This is what we refer to as LO jitter and it is intrinsic to the sampling operation. LO jitter has been analyzed in the literature (e.g. [8]) using conventional stochastic process techniques. The second mechanism is due to the fact that noise at the LO port causes the MOS conductance to fluctuate, and hence producing noise at the output. We call this LO noise. LO noise is independent of sampling, which we now focus on.

LO noise is much more difficult to deal with because the relationship between the LO port and the output port is non-linear and time varying, so frequency domain methods are not applicable. Here, a time domain method based on stochastic differential equation is required. For the single switch sampling mixer, the differential equation is:

$$K(V_G + \sigma\xi_t - V_t)V_D + C\frac{dV_D}{dt} = K(V_G + \sigma\xi_t - V_t)V_S, \tag{7}$$

where $\sigma\xi_t$ represents the white noise at the gate, and $V_S$, $V_D$, $V_G$ are source, drain, and gate voltages respectively. In standard SDE form, if we rewrite the output process $V_D$ as $X_t$, and the input process $V_S$ as $u_t$. Also define MOS conductance $g = K(V_G - V_t)$, we get:

$$dX_t = \frac{g}{C}(u_t - X_t)dt + \frac{K}{C}(u_t - X_t)\sigma dW_t. \quad (8)$$

It is now possible to find $E[X_t]$ and $E[X_t^2]$. The methods involves the concept of quadratic variation and the use of Ito's formula in stochastic calculus [9] [10]. We can show that it is possible to derive a set of ordinary differential equations which govern the behavior of $E[X_t]$ and $E[X_t^2]$. The equations turn out to be:

$$\frac{d}{dt}E[X_t] + \frac{g}{C}E[X_t] = \frac{g}{C}u_t \quad (9)$$

for the mean of the output process, and

$$\frac{d}{dt}E[N_t^2] + \left(\frac{2g}{C} - \frac{\sigma^2 K^2}{C^2}\right) E[N_t^2] = \frac{\sigma^2 K^2}{C^2}(E[X_t] - u_t)^2 \quad (10)$$

for the output noise variance process. From these two equations, analytical solution for output noise variance can be obtained for sampled output. In case where LO waveform is perfectly square, the output noise variance is periodically time varying with the DC term equal to:

$$E[N_t^2] = \frac{A^2}{4} \cdot \frac{\omega^2 C}{K(V_G - V_t)^3} \cdot \sigma^2. \quad (11)$$

Compared to $kT/C$, the magnitude of this noise power is very small, which can be practically ignored. In the case when the LO voltage has a finite fall time, noise variance can become significant. The analytical expression turns out to be:

$$E[N_t^2] = (A^2 - u_t^2)\sqrt{\frac{K}{C}} \left(\frac{T_f}{V_G}\right)^{3/2} \omega^2 \cdot \sigma^2 \cdot 0.443, \quad (12)$$

where $u_t$ is the input process. In fact, LO noise variance is directly related to the slope of the input signal, and it is maximum when the input crosses zero (i.e. when $u_t = 0$). At high frequency, LO noise variance is comparable to $kT/C$. Again, the noise power calculated above is independent of sampling. In the subsampling case, noise power for each sample stays the same, but more noise is folded into the signal band, as in the case for intrinsic noise.

With noise in a single switch sampling mixer thoroughly analyzed, it is now easy to deal with the bottom-plate sampler case. Again, noise contribution is calculated in two parts. As the bottom switch turns off, there are two noise sources in the circuit with combined noise variance equal to $kT/C_s$. As the top switch turns off, an additional amount of intrinsic noise is coupled to the output, but this time the capacitance is smaller. Intrinsic noise in this case is $kT/(C_s \parallel C_p)$. Combining the two, we see the intrinsic noise is approximately $2kT/C_s$, twice as much as the single transistor case. LO noise, on other hand, is much smaller than the single transistor case. There is practically no LO noise as the bottom switch turns off, because LO noise depends on the slope of the input signal, and the voltage level of node Y is fixed to the ground. LO noise is the same as before when the top switch turns off, but since $V_{top}$ is discounted by $C_p/(C_s + C_p)$, its effect is much reduced. Therefore, compared to the single transistor case, LO noise in a bottom-plate sampler is much less a problem than before. Bottom-plate sampling does not affect noise due to jitter at all, so jitter must be considered along noise to get a complete noise performance picture.

## V. Conclusion

We completely analyzed the distortion and noise due to a MOS-based bottom-plate sampling mixer. The method of Volterra series is applied in analysis of harmonic distortion, which combines the effects of continuous time, time varying, and sampling distortions. Frequency domain analysis is applied in the analysis of thermal noise. The method of stochastic differential equation is used to solve for LO noise. These two noise effects need to be combined with LO jitter to give a complete noise picture. The analysis is performed in sampled data domain. Explicit formulas are given to guide the design of bottom-plate sampling mixers.

## References


[1] Armond Hairapetian, "An 81-MHz IF receiver in CMOS," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 12, pp. 1981–1986, December 1996.

[2] P.Y. Chen, A. Rofougaran, K.A. Ahmed, and A.A. Abidi, "A highly linear 1-GHz CMOS downconversion mixer," in *European Solid-State Circuits Conf.*, 1993, pp. 226–227.

[3] Subhajit Sen, *Design of Sampling Mixer and A/D Converter for High IF Digitization*, Ph.D. thesis, University of Waterloo, 1997.

[4] Cynthia Keys, *Low-Distortion Mixers for RF Communications*, Ph.D. thesis, University of California at Berkeley, 1994.

[5] Rober Meyer, "Advanced integrated circuits for communications," Cal VIEW, 1995, UC Berkeley EECS 242 Course Notes.

[6] Wei Yu, Subhajit Sen, and Bosco Leung, "Time varying Volterra series and its application to the disotrtion analysis of a sampling mixer," in *40th Midwest Symposium on Circuits and Systems*, 1997.

[7] Alper Demir, Edward W.Y. Liu, and L. Sangiovanni-Vincentelli, "Time-domain non-Monte Carlo noise simulation for nonlinear dynamic circuits with arbitrary excitations," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 15, no. 5, pp. 493–505, May 1996.

[8] Todd C. Weigandt, Beomsup Kim, and Paul R. Gray, "Analysis of timing jitter in CMOS ring oscillators," in *International Symposium on Circuits and Systems*, 1994, vol. 4, pp. 27–30.

[9] Andrew Heunis, "Stochastic calculus," 1996, University of Waterloo STAT 902 Course Notes.

[10] Ioannis Karatzas and Steven E. Shreve, *Brownian Motion and Stochastic Calculus*, Springer-Verlag, New York, second edition, 1991.